Remarks

Claims 1, 2, 13-17 and 30 have been amended. Claims 5 and 12have been canceled. Reconsideration and allowance of the pending claims are respectfully requested.

Claims Rejection Under 35 U.S.C. 102

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Office Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Office Action has not succeeded in making a *prima facie* case.

Claims 1-7, 10, 12-15 and 30-31

The Office Action rejects claims 1-7, 10, 12-15 and 30-31 under 35. U.S.C. 102 (d) as being anticipated by Kaneko (US PAT. 5,561,672).

Claims 1-7, 10 and 12-15

Claims 1-7, 10 and 12-15 recite an analysis module having a third buffer logic and an analysis device coupled to the third buffer logic, wherein the analysis module is interposed between the second buffer logic and the first buffer logic, and wherein **the second buffer logic transmits a test pattern through the third buffer logic to the first buffer logic to carry out a test of the first memory module**.

The Office Action deems channel unit 15 of Kaneko as the first memory module and deems buffer 41 of Kaneko as the first buffer logic. The Office Action further

deems disk I/F control board 9 of Kaneko as the second memory module and deems the buffer 21 of Kaneko as the second buffer logic. Moreover, the Office Action appears to rely on lines 25-60 of column 2 of Kaneko for the teaching that the second buffer logic transmits a test pattern to the first buffer logic to carry out a test of the first memory module.

From Figures 1A and 1B, buffer 29 of channel I/F control board 13 is interposed between buffer 21 and buffer 41, so that data streams are transmitted from buffer 21 to buffer 41 through buffer 29.

Applicant respectfully submits that lines 25-60 of col. 2 teach that a buffer checking/controlling logic 300, coupled to buffer 29, checks the storage condition of buffer 29 and reports an abnormal data transfer if buffer 29 is not empty after a predetermined data stream read out from buffer 21 has been transferred from buffer 29 to buffer 41. Therefore, lines 25-60 of col. 2 teach that the checking is done in relation to buffer 29, but not in relation to buffer 41.

Further, lines 61-67 of col. 2 and lines 1-7 of col. 3 teach that another buffer checking/controlling logic 25, respectively coupled to buffer 21 and buffer 29, checks whether a data word selected from a data stream in buffer 21 is coincident with a data word selected from in a data stream in buffer 29, so as to determine whether the data streams are transferred by buffer 29 in a normal condition. Again, lines 61-67 of col. 1 and lines 1-7 of col. 3 teach the checking is done in relation to buffer 29, but not in relation to buffer 41.

Therefore, Kanedo does not teach that the second buffer logic transmits a test pattern through the third buffer logic to the first buffer logic to carry out a test of the first memory module, as required by claims 1-7, 10 and 12-15. Therefore, claims 1-7, 10 and 12-15 are allowable. Withdrawal of the present rejection is respectfully requested.

Claims 30-31

For similar reasons proffered for claims 1-7, 10 and 12-15, Kanedo does teach **transmitting the test pattern from the first buffer logic to the second buffer logic, wherein the test pattern is used to carry out a test of the second memory module**, as required by claims 30-31.

In addition, Applicant would like to point out that Kanedo does not teach **storing a test pattern in the first memory array by the first buffer logic in preparation for transmitting** the test pattern **from the first buffer logic to the second buffer logic**, as required by claims 30-31, for the following reasons:

Firstly, the Office Action fails to point out any components of Kanedo that respectively correspond to the first memory array coupled to the first buffer logic and the second memory array coupled to the second buffer logic.

Secondly, Kanedo teaches that buffer 21 transfers data to buffer 41 through buffer 29 upon receiving the data from disk unit 5. In other words, Kanedo does not teach that buffer 21 stores the data in a memory array coupled thereto in preparation for transmitting the data from buffer 21 to buffer 41.

Since Kanedo does not teach each or every limitation of claims 30-31, Kanedo does not anticipate the invention of claims 30-31. Applicant respectfully requests the rejection of claims 30-31 be withdrawn.

Claims 1, 16 and 30

The Office Action rejects claims 1, 16 and 30 under 35. U.S.C. 102 (d) as being anticipated by Oz (US PAT. 6,771,087).

Claim 1

Claim 1, which recites an analysis module having a third buffer logic and an **analysis device coupled to the third buffer logic**, wherein the analysis module is interposed between the second buffer logic and the first buffer logic, and wherein the **second buffer logic transmits a test pattern through the third buffer logic to the first buffer logic** to carry out a test of the first memory module independently of a memory controller, and **the analysis device analyzes a result of the test transmitted from the second buffer logic**, is unanticipated by Kanedo.

The Office Action deems module 101 of Oz as the first memory array of claim 1, and deems buffer 409 as the second buffer logic of claim 1. The Office Action fails to clearly point out which elements of Oz correspond to the first buffer logic, the first memory module, the second memory module and the second memory array of claim 1. The Office Action further cites lines 20-40 of col. 6 after the limitation "a second memory module having a second memory array" of claim 1. Applicant is unable to exactly discern which elements of Oz correspond to the second memory module and the second memory array, simply from lines 20-40 of col. 6.

Based upon the assumption by the Office Action that module 101 corresponds to the first memory array, and that buffer 409 corresponds to the second buffer logic, Applicant respectfully submits that Oz does not teach the invention of claim 1 for the following reasons:

Firstly, since module 101 is coupled to three buffers 401, 411 and 405, it is unclear which buffer corresponds to the first buffer logic of claim 1.

Secondly, if buffer 401 corresponds to the first buffer logic, Oz fails to teach a third buffer interposed between buffer 409 and 401, so that buffer 409 transmits the test pattern through the third buffer to buffer 401. Further, Oz fails to teach an analysis device coupled to the third buffer.

Thirdly, if buffer 405 corresponds to the first buffer logic, then buffer 401 appears to correspond to the third buffer logic. Oz teaches that in the test mode, test bus 400 is used to deliver test outcomes and buffers on input/output ports of the testing module are activated to input the test pattern to the testing module and to output the test result from the testing module (lines 9-11 and 32-38 of col. 6). Therefore, the test result should be transmitted through the test bus, but not through buffer 405. Further, Oz does not provide any details on analysis of the test result, and thus says nothing about an analysis device coupled to the third buffer logic to analyze a result of the test transmitted from the first buffer logic.

Fourthly, if buffer 411 corresponds to the first buffer logic, buffer 401 appears to correspond to the third buffer logic. In lieu of this, Oz does not teach an analysis device

coupled to the third buffer logic to analyze a result of test transmitted from the first buffer logic, for similar reasons stated above.

Since Oz does not teach each or every limitation of claim 1, Oz does not anticipate the invention of claim 1. Applicant respectfully requests the rejection of claim 1 be withdrawn.

Claim 16

Claim 16, which recites a buffer logic of a memory module comprising test logic to **initiate transmission of a test pattern** to another buffer logic of another memory module through the first point-to-point interface to carry out a test of the another memory module independently of a memory controller, is unanticipated by Oz.

It is unclear from the Office Action which elements of Oz correspond to the buffer logic, the memory module, the another buffer logic, and the another memory module of claim 16. Therefore, the following argument is made upon the assumption of claim 1 that module 101 corresponds to the another memory module that carries out the test, and buffer 409 corresponds to the buffer logic that transmits the test pattern to the another memory module to carry out the test.

Based upon the above assumption, Applicant respectfully submits that Oz does not teach that buffer 409 initiates the transmission of the test pattern to the another buffer logic of the another memory module. Instead, Oz teaches the buffer 409 routes the test pattern into the test bus in the test mode (lines 26-29 of col. 6). Therefore, buffer 409 is a router which transfers the test pattern upon receiving the test pattern,

but not an initiator to initiate the transmission of the test pattern. For example, buffer 409 does not command the timing and/or destination address of the transmission.

Since Oz does not teach each or every limitation of claim 16, Oz does not anticipate the invention of claim 16. Applicant respectfully requests the rejection of claim 1 be withdrawn.

Claim 30

Claim 30, which recites **storing a test pattern in the first memory array by the first buffer logic** in preparation for transmitting the test pattern from the first buffer logic to the second buffer logic, wherein the test pattern is used to carry out a test of the second memory module independently of a memory controller, is unanticipated by Oz.

It is unclear from the Office Action which elements of Oz correspond to the first buffer logic, the first memory array, the first memory module, the second buffer logic, the second memory array and the second memory module. Therefore, the following argument is made upon the assumption of claim 1 that module 101 corresponds to the second memory module that carries out the test, and buffer 409 corresponds to the first buffer logic that transmits the test pattern to the second memory module to carry out the test.

Based upon the above assumption, Oz does not teach buffer 409 stores the test pattern in the first memory array in preparation for transmitting the test pattern from buffer 409 to module 101. Oz teaches test pattern is input from I/O port 407 and then is routed through buffer 409 to module 101 (lines 25-31 of col. 6). However, Oz

does not provide any details on where the test pattern is stored and which element stores the test pattern before the test pattern is transmitted from buffer 409 to module 101.

Since Oz does not teach each or every limitation of claim 30, Oz does not anticipate the invention of claim 30. Applicant respectfully requests the rejection of claim 30 be withdrawn.

Claims Rejections Under 35 U.S.C. 103(a)

The Office Action rejected claims 8-11, 16-24 and 25-29 under 35 U.S.C. 103 as being unpatentable over Kanedo.

Claims 8-11

Claims 8-11 include claim 1 as a base claim and are thus allowable for at least the reasons mentioned above. Applicant respectfully requests reconsideration and withdrawal of the present rejection.

Claims 16-24

As discussed in M.P.E.P 2143.03, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claims 16-24, which recite a buffer logic of a memory module comprising test logic to **initiate transmission of a test pattern** to another buffer logic of another

memory module through the first point-to-point interface to carry out a test of the another memory module independently of a memory controller, is neither taught nor suggested by Kanedo.

The Office Action appears to deem that buffer 21 corresponds to the buffer logic that transmits the test pattern and buffer 41 corresponds to the another buffer logic to receive the test pattern for testing.

Based upon the above, Kanedo teaches that the transmission of data from disk 5 to memory 1 is instructed by the channel instruction word from memory 1, which determines the desire disk address for data transmission (lines 3-5 and 11-14 of col. 10). During the transmission, data read from disk 5 is transmitted to memory 1 via buffer 21, buffer 29 and buffer 41. Therefore, Kanedo teaches that buffer 21 is a relayer to relay the data on the path from disk 5 to memory 1, but not an initiator to initiate the transmission to memory 1.

Since Kanedo does not teach or suggest each or every limitation of claims 16-24, claims 16-24 are patentable over Kanedo. Applicant respectfully requests the rejection of claims 16-24 be withdrawn.

Claims 25-29

As discussed in M.P.E.P 2143.03, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claims 25-29, which recite transmitting a command to the first buffer logic to **cause the first buffer logic to transmit a test pattern through the third buffer logic to the second buffer logic,** wherein the test pattern is used to **carry out a test of the second memory module** independently of a memory controller, is neither taught nor suggested by Kanedo.

For similar reasons proffered for claim 1, Kanedo does not teach that buffer 21 transmits a test pattern through buffer 29 to buffer 41 to carry out a test of module 15.

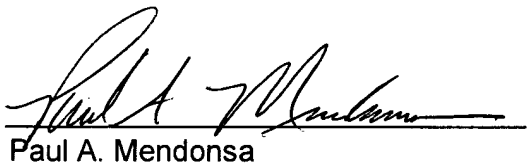
Since Kanedo does not teach or suggest each or every limitation of claims 25-29, claims 25-29 are patentable over Kanedo. Applicant respectfully requests the rejection of claims 25-29 be withdrawn.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that the application is in condition for allowance. Reconsideration is requested, and allowance of the pending claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities, which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,



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